Resource Utilization Optimized Design Method for Matched Filter of PSS Searcher

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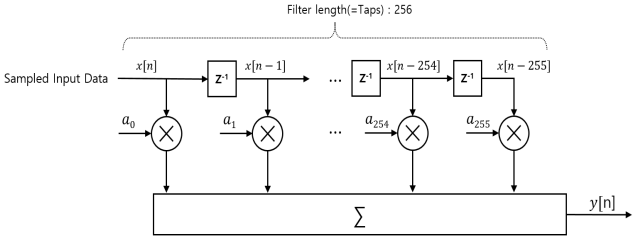
Abstract— **In LTE(Long-Term Evolution) system, UE(User Equipment) performs synchronization processing with a specific cell to communicate. In that processing, the UE uses a matched filter to filter PSS(Primary Synchronization Signal) from downlink signals sent from the cell. There are various ways to design such a matched filter. In the most native design of the matched filter, the number of multipliers is required as much as a number of the taps which means filter length. If resources are limited, that is a very inefficient design approach. Therefore, we proposed filter design method to significantly reduce the number of multipliers in the matched filter by utilizing the difference of between sampling rate and operating clock frequency. When using FPGA resources for designing the filter, The filter design method proposed in this paper reduced the LUT(look-up table) utilization by 55.2% to 6.22%, the FF(flip-flop) utilization decreased by 24.95% to 4.44%, and the BRAM utilization decreased by 42.65% to 13.05% than the Natively design method.**

Keywords; Long-Term Evolution; Primary Synchronization Signal; Matched filter;

I. INTRODUCTION

UE (e.g. mobile phone) uses a matched filter to extract a specific signal which is used for synchronizing with the LTE signal. The matched filter used in the UE can be implemented as a digital filter, especially FIR(Finite Impulse Response) digital filter that performs filtering with finite input samples. Therefore, for the filtering process in the FIR filter, the LTE signals are converted into finite samples. The finite samples of LTE signal are transferred to the matched filter and performed filtering by using multiplication and accumulation(MAC) operation with coefficient values. Fig.1 shows the matched filter's filtering operation. Whenever a new input sample comes in, the previously entered samples are shifted side by side and the matched filtering is progressed through MAC operation. At this time, the length of the FIR filter is called 'Taps' and the number of the taps is equal to the number of multipliers used in the matched filter.

If the matched is designed natively, multipliers are needed as much as the number of the taps. However, it is very inefficient to design a filter through a large number of multipliers when the filter needs to be designed with limited resources. In this paper, we proposed a design method to minimize the number of multipliers by using the difference between the incoming clock frequency of the LTE sample signals and the operating clock frequency of the matched filter.



$$y[n] = a_0x[n] + a_1x[n-1] + \ \ldots + a_{254}x[n-254] + a_{255}x[n-255]$$

$$y[n] = \sum_{k=0}^{N-1} a_k x[n-k] \qquad a_k : coefficient$$

Figure 1. MAC processing of Matched filter

II. BACKGROUND

LTE(Long-Term Evolution) is a high-speed wireless mobile communication technology that exchanges data [1].

LTE generally uses FDD(Frequency Division Duplex), which is a method of separating and transmitting signals in both directions. it is divided into 'downlink', which is information transmission from base station to device, and 'uplink', which is information transmission from device to base station. Among them, we focused on the downlink process. When the UE is turned on, network information transmitted from nearby base stations is received, attempt to access the network of the base station. Fig.2 shows each base station has there own service coverage area, which is called a 'Cell'. The UE in the specific cell try to search a downlink signal. That is called 'Cell Search Procedure'.

The first step of the cell search procedure is synchronizing

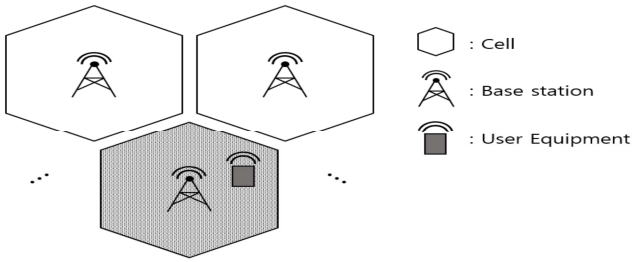


Figure 2. Cell and User equipment

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with the downlink signal sent from the cell. Cell periodically transmits downlink signal in units of 1 frame(10ms), and a synchronization signal is included in this downlink signal. The UE finds out information about a specific cell through finding a synchronization signals and synchronizing with that signal [2].

The first synchronization signal in the cell search procedure is the Primary Synchronization Signal(PSS). Fig.3 shows positions of PSS in the downlink signal. PSS exists twice in the frame(10ms), and the same signal is broadcasted. The downlink signal is composed of 10 subframes(1ms) divided by 10 equals 1 frame time length(10ms), and the PSS are present in subframe0 and subframe5. Therefore, since the same PSS signal comes in every 5ms, it can be extracted to check the 5ms timing range of the downlink signal sent from the cell.

III. PROPOSED SCHEME

In this paper, the LTE system is assumed as follows. The ADC sampling rate of the downlink signal is 3.84MHz, and the operating frequency of the matched filter is based on 61.44MHz. Therefore, the total number of downlink signal samples in 1 frame is 38400 samples. The taps number of the matched filter is set to 256. So, when the matched filter with 256 taps is designed natively, the filter has 256 multipliers.

In the general LTE system, the clock frequency of the matched filter is much faster than the sampling rate. Since the filter operation clock frequency in this paper is 61.44MHz, it is 16 times faster than the sampling rate(3.84MHz). i.e. It means that the filtering process can be performed 16 times before the next input sample comes in.

To utilize this point, instead of using a matched filter with 256 multipliers, a partial matched filter composed of 16 multipliers is constructed. Therefore, the matched filter calculates partial MAC operation corresponding to 16 taps with

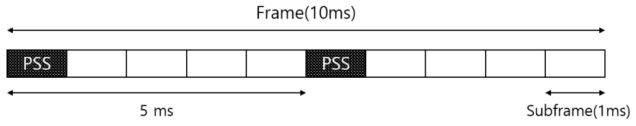

Figure 3. Positions of PSS in downlink signal

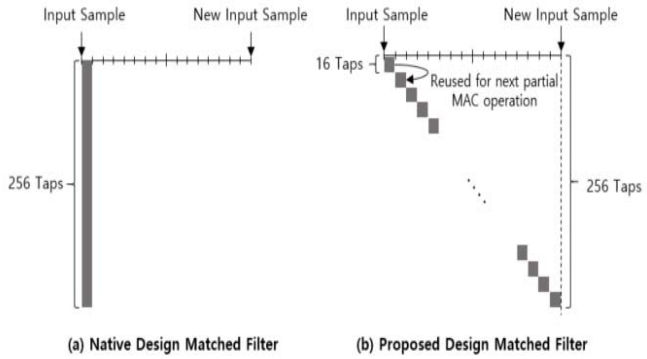

Figure 4. Comparison filtering process of (a) native design and (b) proposed design matched filters

TABLE I. COMPARISON RESOURCE UTILIZATION

Filter Design	Utilization (%)		
	LUT	***FF***	***BRAM***
Native design	55.20	24.95	42.65
Proposed design	6.22	4.44	13.05

a 61.44 MHz clock frequency. And we can reuse 16 times the partial matched filter to complete fully MAC operation (256 taps) until the next sample comes in. i.e. It means that with only the matched filter composed of 16 taps, the operation corresponding to 256 taps can be completed until the next input sample comes. The proposed scheme can be seen in Fig.4-(b).

IV. EVALUATION

To compare the resource usage on an FPGA(field programmable gate array), the native design filter and the proposed design filter designed by RTL code(e.g.Verilog) were implemented on the FPGA. The metric for comparison was set to a look-up table (LUT), flip-flop (FF), and block random access memory (BRAM). The FPGA was used the ZU9EG(XCZU9EG-2FFVB1156E) model in this experiment. The available amount of resource unit in the FPGA has LUT: 274080, FF: 548160, and BRAM: 912. Table 1 shows the results of resource utilization. When comparing the resource utilization rate with the native design filter and the proposed design filter, the proposed design filter decreased by 48.98% for LUT, 20.51% for FF, and 29.6% for BRAM than native design filter.

V. CONCLUSION

In this work, we proposed a method to design a matched filter efficiently under limited resources. The proposed PSS searcher design scheme uses the difference of filter operating clock frequency and input sampling rate. the filtering operation needs to be completed only before the next signal comes in. So, only a partial operating filter is used to several times partial filtering operation to finish the whole filtering operation before the next input sample comes in. Since the PSS searcher is designed by partial filter, the overall resource utilization can be reduced.

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